Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	6	("5504670" "5682530" "5740357").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:21
L3	47	("5504670" "5682530" "5740357").uref.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:48
L4	3	l3 and (default near3 policy)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:49
L5	30	((hierarch$4 near6 (fault or failure or error or debug$4 or event))with (manag$5 or control$4 or protect$4 or handl$4))same default	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:40
L6	24	((hierarch$4 near6 (fault or failure or error or debug$4 or event))with (manag$5 or control$4 or protect$4 or handl$4))same (default near3 (polic$3 or rul$2))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:55
L7	42	("5689668" "5559945").uref.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:48
L8	0	l7 and (default near3 policy)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 13:20
L9	22111	"713"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 13:19

L10	4	l9 and (((hierarchical near4 manag$5)same (fault or event or error or default)) same (configur$4 or program$5 or alter$4 or chang$4 or select$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 13:19
L11	607	((hierarch$4 near6 (fault or failure or error or event))with (manag$5 or control$4 or protect$4 or handl$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:59
L12	24	l11 and ((default near3 (polic$3 or rul$2)) same (configur$5 near3 (polic$3 or rul$2)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:31
L13	0	"6721947.uref"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:31
L14	0	"6721947".uref.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:31
L15	2	"6721947".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:47
L16	0	(default near5 ((event or fault or failure)near3 ploic$3))same ((configurable or program$5 or alter$4)near2 polic$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:49
L17	0	(default near5 ((event or fault or failure)near3 ploic$3))with ((configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5)near2 default)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:51

L18	0	(default near5 ((event or fault or failure)near3 ploic$3))with ((configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:51
L19	0	(((event or fault or failure)near3 ploic$3))with ((configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5))same (default near2 polic$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:53
L20	0	((hierarchical or hierarch$3)near3 (((event or fault or failure)near3 (manag$5 or control$4 or repson$4))))with ((configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5))same (default near2 polic$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 10:56
L21	0	(((hierarchical or hierarch$3)near3 (event or fault or failure))with (manag$5 or control$4 or repson$4))with ((configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5)same (default near2 polic$2))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 12:32
L22	0	(((fault or failure or error)near3 recover$3) with ((hierarchical or hierarch$3)near4 (manag$5 or control$4 or repson$4)))same (configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5)same (default near2 polic$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 12:36
L23	0	((fault or failure or error)near3 recover$3) same ((hierarchical or hierarch$3)near4 (manag$5 or control$4 or repson$4))same (configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5)same (default near2 polic$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 12:37
L24	1	((fault or failure or error)near3 recover$3) same ((hierarchical or hierarch$3)near4 (manag$5 or control$4 or repson$4))same (configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5)and (default near2 polic$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 12:39

L25	0	(((fault or failure or error)near3 recover$3) same ((hierarchical or hierarch$3)near4 (manag$5 or control$4 or repson$4)))and ((configurable or program$5 or alter$4 or chang$4 or modify$3 or modifi$5)same (default near2 polic$2))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 12:38
L26	29272	"707"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 13:19
L27	35	l26 and (((hierarchical near4 manag$5)same (fault or event or error or default)) same (configur$4 or program$5 or alter$4 or chang$4 or select$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 13:19
L28	4	l27 and (default near3 policy)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 13:24
L29	23	l27 and (default)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 13:24

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
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- Capitalize proper nouns to search for specific people, places, or products.

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- Enclose a phrase in double quotes to search for that exact phrase.

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  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

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  ```

- Exclude pages by using a - if a search term must not appear on a page.

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Terms used **hierarchical fault** or **event default** Found **9,998** of **161,645**

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1 Performance analysis for hierarchical multirate loss networks
Ben-Jye Chang, Ren-Hung Hwang
February 2004 **IEEE/ACM Transactions on Networking (TON)**, Volume 12 Issue 1
Full text available: pdf(523.27 KB) Additional Information: full citation, abstract, references, index terms

The reduced load approximation technique has been extensively applied to flat networks, but the feasibility of applying it to hierarchical network model has seldom been described. Hierarchical routing is essential for large networks such as the Internet inter/intra-domain routing hierarchy and the Private Network to Node Interface (PNNI) standard. Therefore, this paper proposes an efficient and accurate analytical model for evaluating the performance of hierarchical networks with multiple classe ...

Keywords: hierarchical routing, loss networks, performance analysis, private network to node interface (PNNI), reduced load approximation

2 Session 1B: Approximation algorithms for hierarchical location problems
C. Greg Plaxton
June 2003 **Proceedings of the thirty-fifth annual ACM symposium on Theory of computing**
Full text available: pdf(224.38 KB) Additional Information: full citation, abstract, references, index terms

We formulate and (approximately) solve hierarchical versions of two prototypical problems in discrete location theory, namely, the metric uncapacitated *k*-median and facility location problems. Our work yields new insights into hierarchical clustering, a widely used technique in data analysis. First, we show that every metric space admits a hierarchical clustering that is within a constant factor of optimal at every level of granularity with respect to the average (squared) distance object ...

Keywords: discrete location theory, hierarchical clustering

3 Hierarchical planarity testing algorithms
Thomas Lengauer
July 1989 **Journal of the ACM (JACM)**, Volume 36 Issue 3
Full text available: pdf(2.55 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Using hierarchical definitions, one can describe very large graphs in small space. The blow-up from the length of the hierarchical description to the size of the graph can be as large as exponential. If the efficiency of graph algorithms is measured in terms of the length of the hierarchical description rather than in terms of the graph size, algorithms that do not

Terms used **hierarchical event or fault default** Found **38** of **161,645**

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Relevance scale

1 High level hierarchical fault simulation techniques

William A. Rogers, Jacob A. Abraham

March 1985 **Proceedings of the 1985 ACM thirteenth annual conference on Computer Science**

Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents techniques for simulating directly from a hierarchical circuit description without flattening to the level of primitives. An overview of traditional fault simulation techniques is followed by details of the hierarchical techniques. The fault model is shown to be decoupled from the simulator programs through the use of a fault library. The fault library allows the user to mix both functional and technology-dependent fault models, which allows fault simulation and conseque ...

2 Diagnostic and Detection Fault Collapsing for Multiple Output Circuits

Raja K. K. R. Sandireddy, Vishwani D. Agrawal

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 2**

Full text available: pdf(148.29 KB) Additional Information: full citation, abstract

We discuss fault equivalence and dominance relations for multiple output combinational circuits. The conventional definition for equivalence says that "Two faults are equivalent if and only if the corresponding faulty circuits have identical output functions". This definition, which is based on indistinguishability of the faults, is extended for multiple output circuits as "Two faults of a Boolean circuit are equivalent if and only if the pair of the output functions is identical at each output ...

3 Parallel and distributed systems and networking: Cycle embedding in faulty hierarchical cubic networks

Jung-Sheng Fu, Gen-Huey Chen

March 2002 **Proceedings of the 2002 ACM symposium on Applied computing**

Full text available: pdf(470.97 KB) Additional Information: full citation, abstract, references, index terms

A hierarchical cubic network was proposed as an alternative to the hypercube. We use HCN (n) to denote the hierarchical cubic network that contains 2^n n-dimensional hypercubes. In this paper, using Gray codes, we construct fault-free hamiltonian cycles in an HCN(n) with n-1 link faults. Since the HCN(n) is regular of degree n+1, the result is optimal. We also construct longest fault-free cycles of length 2^{2n}-1 in an HCN ...

Keywords: fault-tolerant embedding, gray code, hamiltonian cycle, hierarchical cubic network, hypercube

4 Session 9D: new approaches to at-speed BIST and diagnosis: Diagnosis of interconnect faults in cluster-based FPGA architectures
Ian Harris, Russell Tessier
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(60.64 KB) Additional Information: full citation, abstract, references, citings

Fault diagnosis has particular importance in the context of field programmable gate arrays (FPGAs) because faults can be avoided by reconfiguration at almost no real cost. Cluster-based FPGA architectures, in which several logic blocks are grouped together into a coarse-grained logic block, are rapidly becoming the architecture of choice for major FPGA manufacturers. The high density interconnect found within clusters greatly complicates the problem of FPGA diagnosis. We propose a technique for ...

5 Interconnect testing in cluster-based FPGA architectures
Ian G. Harris, Russell Tessier
June 2000 **Proceedings of the 37th conference on Design automation**
Full text available: pdf(276.60 KB) Additional Information: full citation, abstract, references, citings, index terms

As IC densities are increasing, cluster-based FPGA architectures are becoming the architecture of choice for major FPGA manufacturers. A cluster-based architecture is one in which several logic blocks are grouped together into a coarse-grained logic block. While the high density local interconnect often found within clusters serves to improve FPGA utilization, it also greatly complicates the FPGA interconnect testing problem. To address this issue, we have developed a hierarchical approach ...

Keywords: field-programmable gate arrray, hierarchical test, interconnect testing

6 A practical nonmonotonic theory for reasoning about speech acts
Douglas Appelt, Kurt Konolige
June 1988 **Proceedings of the 26th annual meeting on Association for Computational Linguistics**
Full text available: pdf(693.58 KB) Publisher Site Additional Information: full citation, abstract, references, citings

A prerequisite to a theory of the way agents understand speech acts is a theory of how their beliefs and intentions are revised as a consequence of events. This process of attitude revision is an interesting domain for the application of nonmonotonic reasoning because speech acts have a conventional aspect that is readily represented by defaults, but that interacts with an agent's beliefs and intentions in many complex ways that may override the defaults. Perrault has developed a theory of speec ...

7 An optimized ATPG
Samiha Mourad
June 1980 **Proceedings of the 17th conference on Design automation**
Full text available: pdf(361.18 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a hierarchical approach to the detection of the critical faults of a digital board, i.e., those most likely to occur. The failure probabilities of the nodes of a board are estimated and used as weights in selecting the nodes for fault detection. The study has indicated both a saving in pattern generation and a higher fault detection per pattern. This approach introduces a new definition of fault coverage. The approach is also applicable to analog circuits. In addition, ...

8 A hierarchical approach test vector generation
S. J. Chandra, J. H. Patel

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(653.38 KB) Additional Information: full citation, abstract, references, citings, index terms

Given a combinational network and a specific stuck-at fault to be detected, there are several approaches to generating a test vector. However, most of these approaches fail to exploit the hierarchy inherent in any complex digital design. This paper presents a hierarchical approach to test vector generation. HIPODEM: A test generation system based on this approach is presented. General procedures to perform forward implication and backtracing in a hierarchical framework are discussed in deta ...

9 A hierarchical multicast monitoring scheme

Joerg Walz, Brian Neil Levine

November 2000 **Proceedings of NGC 2000 on Networked group communication**

Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, index terms

Deployment of multicast routing services in corporate networks and Internet Service Providers is still tentative. Among other problems, there is a lack of monitoring and management tools and systems. Previous work in multicast management has failed to address the scalability problem present in multicast fault isolation and reporting. We propose a hierarchical, passive monitoring scheme, HPMM, that relies on a series of pre-deployed, self-organized monitoring daemons. With HPMM, fault message ...

10 Morphology, phonology, syntax: Structure sharing in lexicalized tree-adjoining grammars

K. Vijay-Shanker, Yves Schabes

August 1992 **Proceedings of the 14th conference on Computational linguistics - Volume 1**

Full text available: pdf(441.20 KB) Additional Information: full citation, abstract, references, citings

We present a scheme for efficiently representing a lexicalized tree-adjoining grammar (LTAG). The proposed representational scheme allows for structure-sharing between lexical entries and the trees associated with the lexical items. A compact organization is achieved by organizing the lexicon in a hierarchical fashion and using inheritance as well as by using lexical and syntactic rules.While different organizations (Flickinger, 1987; Pollard and Sag, 1987; Shieber, 1986) of the lexicon have bee ...

11 Logic simulation and fault analysis of a self-checking switching processor

H. Y. Chang, R. C. Dorr, R. A. Elliott

June 1972 **Proceedings of the 9th workshop on Design automation**

Full text available: pdf(542.26 KB) Additional Information: full citation, abstract, references, index terms

During an exploratory study in the design of a stored program processor for an electronic switching system, the need for logic simulation for design verification was evident [1]. The advantages of using logic simulation concurrent with hardware design are many. This paper will discuss logic simulation and fault analysis work undertaken while designing a self-checking switching processor. The logic simulation and fault analysis were implemented on an IBM/360 model 67 executing a s ...

12 Experience reports: case studies: Fault-tolerance in a distributed management system: a case study

Robert Smeikal, Karl M. Goeschka

May 2003 **Proceedings of the 25th International Conference on Software Engineering**

Full text available: pdf(864.67 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

Our case study provides the most important conceptual lessons learned from the implementation of a Distributed Telecommunication Management System (DTMS), which controls a networked voice communication system. Major requirements for the DTMS are fault-tolerance against site or network failures, transactional safety, and reliable

persistence. In order to provide distribution and persistence both transparently and fault-tolerant we introduce a two-layer architecture facilitating an asynchronous re ...

13 Analysis of a composite performance reliability measure for fault-tolerant systems
Lorenzo Donatiello, Balakrishna R. Iyer
January 1987 **Journal of the ACM (JACM)**, Volume 34 Issue 1

Full text available: pdf(1.43 MB) Additional Information: full citation, abstract, references, citings, index terms

Today's concomitant needs for higher computing power and reliability has increased the relevance of multiple-processor fault-tolerant systems. Multiple functional units improve the raw performance (throughput, response time, etc.) of the system, and, as units fail, the system may continue to function albeit with degraded performance. Such systems and other fault-tolerant systems are not adequately characterized by separate performance and reliability measures. A composite measure for the pe ...

14 Internet-Based Collaborative Test Generation with MOSCITO
A. Schneider, K. Diener, E. Ivask, J. Raik, R. Ubar, P. Miklos, T. Cibáková, E. Gramatová
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(419.63 KB) Publisher Site Additional Information: full citation, abstract

This paper offers an Internet-based environment forenhancing problem-specific design flows with test patterngeneration and fault simulation capabilities. AutomaticTest Pattern Generation (ATPG) and fault simulation toolsat structural and hierarchical levels available at geographicallydifferent places running under the virtual environmentusing the MOSCITO system are presented. Thesetools can be used separately, or in multiple applications,for test pattern generation of digital circuits. In order ...

15 Applications of qualitative modeling to knowledge-based risk assessment studies
Gautam Biswas, Kenneth A. Debelak, Kazuhiko Kawamura
June 1989 **Proceedings of the second international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1**

Full text available: pdf(729.63 KB) Additional Information: full citation, abstract, references, citings, index terms

Risk assessment of technological processes (chemical and power plants, electro-mechanical systems) is a complex process that requires enumeration of all possible failure modes, their probability of occurrence, and their consequences. Traditionally such studies have been performed by a committee of expert engineers with diverse backgrounds. This paper discusses the use of qualitative modeling techniques based on deriving behavior from structural descriptions and causal reasoning to aid autom ...

16 Session: Synchronization as a framework for distributed system fault-tolerance design
Alexander B. Romanovsky
September 1992 **Proceedings of the 5th workshop on ACM SIGOPS European workshop: Models and paradigms for distributed systems structuring**

Full text available: pdf(531.94 KB) Additional Information: full citation, abstract, references

We shall regard a computer system as a whole which comprises software, hardware and mixed components each of which can, in its turn, present a system. Then the entire system is a multilevel hierarchy.The purpose of this paper is to single out and generalize about the essential features and properties of synchronization and to argue in favour of the idea of designing and developing fault-tolerance (FT) for distributed systems on the basis of a multilevel synchronization system. Getting aware of a ...

17 A hierarchical symptom classification for model based causal reasoning
C. Lee, P. Liu, S. Clark, M. Y. Chiu
June 1988 **Proceedings of the first international conference on Industrial and**

engineering applications of artificial intelligence and expert systems - Volume 1

Full text available: pdf(622.51 KB) Additional Information: full citation, abstract, references, index terms

Model based causal reasoning has been widely used for physical systems diagnosis. The system fault is localized with the causal relation of system structure and behavior. In such applications, if the system fault is not localized with the observed behavior, then a subsequent observation is made. This research studies a hierarchical symptom classification for guiding a subsequent observation in model based causal reasoning. The diagnostic symptoms are mapped to the system fu ...

18 Circuit effects in static timing: VeriCDF: a new verification methodology for charged device failures

Jaesik Lee, Ki-Wook Kim, Sung-Mo Kang

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

A novel tool for full-chip verification is reported for CDM-ESD protection. Until recently, ESD protection has been simulated in device level, leading to the well known limitations on capturing global features such as the power protection circuits and package parasitics. In practice, fatal failures occur due to unexpected discharged paths in multi-power supply chips, which can only be verified by chip-level simulation. Associated with the new concept of macromodelling, hierarchical approach prov ...

Keywords: modeling, reliability, simulation

19 Reliability and performance of hierarchical RAID with multiple controllers

Sung Hoon Baek, Bong Wan Kim, Eui Joung Joung, Chong Won Park

August 2001 **Proceedings of the twentieth annual ACM symposium on Principles of distributed computing**

Full text available: pdf(663.16 KB) Additional Information: full citation, abstract, references, index terms

Redundant arrays of inexpensive disks (RAID) offer fault tolerance against disk failures. However a storage system having more disks suffers from less reliability and performance. A RAID architecture tolerating multiple disk failures shows severe performance degradation in comparison to the RAID Level 5 due to the complexity of implementation. We present a new RAID architecture that tolerates at least three disk failures and offers similar throughout to the RAID Level 5. We call it the hierar ...

Keywords: Markov process, hierarchical RAID, high reliability, three-failure-tolerant array

20 An approach to fast hierarchical fault simulation

Akira Motohara, Motohide Murakami, Miki Urano, Yasuo Masuda, Masahide Sugano

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Full text available: pdf(656.08 KB) Additional Information: full citation, abstract, references, index terms

We present an approach to hierarchical fault simulation which generates several simulation-models of one circuit and carries out simulation for each. Fault insertion and simulation-model generation is done automatically. Switch-level simulation which utilizes look-up tables is as fast as gate-level simulation. Experimental results show that using behavioral description and switch-level truth tables is effective to improve simulation speed.